LAND PATTERN RECOMMENDATIONS FOR HV CERAMIC CAPACITORS

INTRODUCTION

Tables I and II† illustrate recommended land pattern / solder pad layout dimensions for surface mount MLCC capacitors and capacitor assemblies. They have been derived in part from the "Surface Mount Design and Land Pattern Standard IPC 7351 and it is recommended that the engineer reference this Institute for Interconnection and Packaging Electronic Circuits (IPC) document and the notes below for additional information.

As of this writing, there are no established standards currently available that cover land pattern recommendations for "J" lead and "L" lead surface mount configurations. Consequently, IPC 7351 methodology was utilized as the basis for establishing the recommended dimensions included with this application note.

GENERAL CONSIDERATIONS

Although these recommendations should help provide the basis for a reliable soldering process, they may not be applicable to all situations and as such should not be considered a guarantee against inadequate results. Consequently, it becomes the engineer's responsibility to confirm results and make adjustments where necessary to accommodate specific conditions and design requirements. Other factors that can influence the outcome and should be considered when establishing a suitable pad layout are as follows:

- Land pattern dimensions shown in Table 2 reflect nominal capacitor sizes and at those dimensions are designed to allow for 0.010" clearance between the outer pad perimeter and the tab lead. Any changes deemed necessary due to land pattern maximum / minimum capacitor tolerances are at the discretion of the engineer.

- A wave soldering process is discouraged for capacitor package sizes 1812 and up due to their larger mass. In these situations, a wave process is generally insufficient in providing adequate preheat for the capacitor and consequently, these package sizes are more susceptible to microfracturing.

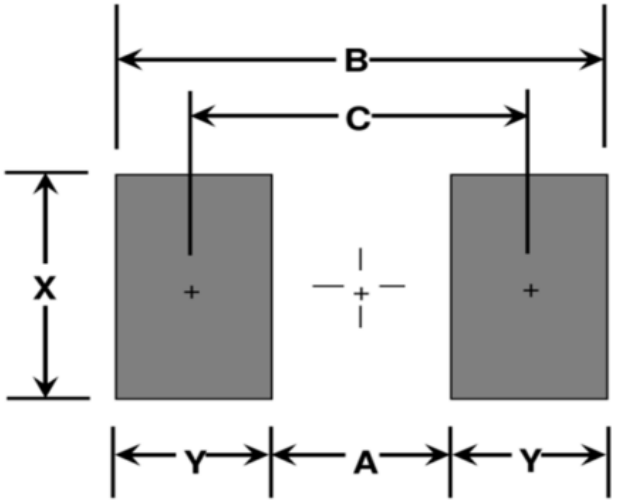
- When utilizing a wave soldering process to install a surface mount chip capacitor, it is recommended that the pad width be narrower than the width of the capacitor to lessen the risk of capacitor microfracturing due to board twisting or distortion. This methodology will generally restrict the solder fillet to the end termination and change the appearance of what is commonly considered to be a typical solder joint, but this difference is generally viewed as purely cosmetic and should in no way diminish the reliability of the solder joint or the functionality of the capacitor.

- When utilizing a wave soldering process to install a surface mount capacitor, it is recommended that the capacitors be aligned perpendicular to the direction of the solder wave. Orientation in a direction that is parallel with the solder wave may impede the flow of solder, may increase the likelihood of encountering cold or insufficient solder joints on the trailing edge of the device and may require the need for a dual wave process to compensate.

- Where there are concerns over board flexure, it is recommended that surface mount chip capacitors be positioned in those regions of the board where they are less likely to encounter this type of mechanical stress. Of particular concern would be those areas in close proximity to larger components and around the outside perimeter of the PWB. These locations should be avoided if possible and / or the use of board stiffeners should be considered. In addition, surface mount chips should be oriented parallel to any potential bend axis, especially in those applications where there tends to be a major difference in the aspect ratio of the PWB. (ie. Typical lighting ballast circuit boards)

- Adequate cleanliness and proper isolation of the terminations is especially critical for high voltage surface mount capacitors. Failure to meet these prerequisites may increase the risk for an arc-over condition and the engineer may want to consider the use of a leaded surface mount assembly, or incorporate either a slot or groove in the area between the solder pads to allow adequate flow of cleaning fluids and potting compounds.

RECOMMENDED PAD SIZES

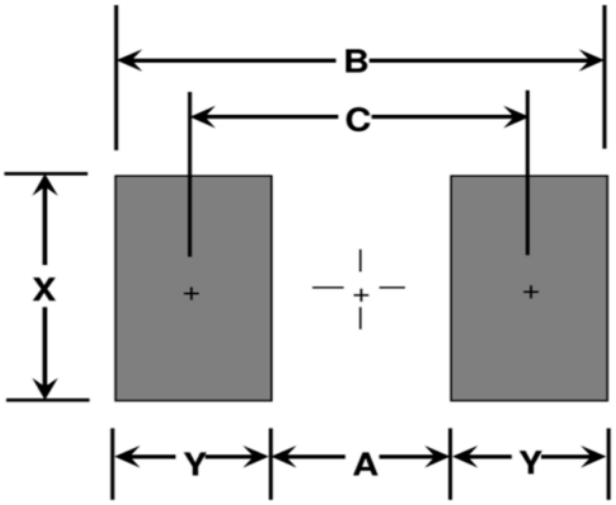


Ref. IPC 7351

HV Chip Size	Convection / Reflow Solder Process					Wave Solder Process				
	X	Y (Typ.)	A	B (Ref.)	C (Ref.)	X	Y (Typ.)	A	B (Ref.)	C (Ref.)
HV1515	0.205	0.080	0.075	0.205	0.120	0.170	0.080	0.075	0.205	0.120
HV1812	0.175	0.100	0.075	0.240	0.140	0.140	0.100	0.075	0.240	0.140
HV1825	0.310	0.100	0.075	0.240	0.140	Wave solder process may not be suitable for HV1515 and HV1812 sizes and is not recommended for all other package sizes				
HV2020	0.260	0.100	0.075	0.260	0.170					
HV2225	0.310	0.100	0.080	0.280	0.180					
HV2520	0.260	0.120	0.075	0.310	0.190					
HV3333	0.400	0.130	0.140	0.400	0.270					
HV3530	0.370	0.130	0.160	0.420	0.290					
HV4040	0.470	0.130	0.210	0.470	0.340					
HV4540	0.470	0.130	0.260	0.520	0.390					
HV5440	0.470	0.130	0.350	0.610	0.480					
HV5550	0.570	0.130	0.360	0.620	0.490					
HV6560	0.670	0.130	0.460	0.720	0.590					
HV7030	0.370	0.130	0.510	0.770	0.640					
HV9040	0.470	0.130	0.710	0.970	0.840					
HV11050	0.570	0.130	0.910	1.170	1.040					
HV13060	0.670	0.130	1.110	1.370	1.240					

Table I – HV Surface Mount Chip Capacitors†

†The guidelines presented in Table I and Table II are for reference only, please refer to IPC 7351 for precise recommendations. It is left up to the design engineer to determine whether or not dimensions herein are suitable for the Application based on actual capacitor dimensions and system considerations. CalRamic Technoligies LLC is not responsible for any damage caused my misuse or misinterpretation of this data.



Ref. IPC 7351

HV Chip Size	J - Lead					L - Lead				
	X	Y (Typ.)	A	B (Ref.)	C (Ref.)	X	Y (Typ.)	A	B (Ref.)	C (Ref.)
SM01	0.200	0.107	0.075	0.225	0.118	0.200	0.105	0.095	0.305	0.200
SM02	0.200	0.112	0.075	0.280	0.168	0.200	0.110	0.140	0.360	0.250
SM03	0.200	0.117	0.101	0.335	0.218	0.200	0.115	0.185	0.415	0.300
SM10	0.200	0.192	0.075	0.390	0.198	0.200	0.190	0.230	0.610	0.420
SM04	0.300	0.192	0.075	0.440	0.248	0.300	0.190	0.280	0.660	0.470
SM11	0.200	0.192	0.106	0.490	0.298	0.200	0.190	0.330	0.710	0.520
SM05	0.400	0.192	0.156	0.540	0.348	0.400	0.190	0.380	0.760	0.570
SM06	0.500	0.192	0.256	0.640	0.448	0.500	0.190	0.480	0.860	0.670
SM07	0.600	0.192	0.356	0.740	0.548	0.600	0.190	0.580	0.960	0.770
SM13	0.300	0.192	0.406	0.790	0.598	0.300	0.190	0.630	1.010	0.820
SM14	0.400	0.192	0.606	0.990	0.798	0.400	0.190	0.830	1.210	1.020
SM15	0.500	0.192	0.856	1.240	1.048	0.500	0.190	1.080	1.460	1.270
SM16	0.600	0.192	1.006	1.390	1.198	0.600	0.190	1.230	1.610	1.420

Table 2 – SM Surface Mount Capacitor Assemblies†

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